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EXAMINER	
BEDNASH, JOSEPH A	

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2461	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/583,167	KIM ET AL.	
	Examiner	Art Unit	
	Joey Bednash	2461	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 June 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1, 2 and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the structure for transferring the modulation methods analyzed by the channel decoder to the QAM demapper must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: Para [0014] includes a reference to Fig. 4. It appears that this is a typographical error since the reference is with regards to time delay and Fig. 4 is a QPSK constellation. The specification contains several typographical errors, for instance in Para [0007] the term "describinges" is used. It is understood by examiner to be either describes or describing, but should be clarified.

Appropriate correction is required.

Claim Objections

4. Claim 1 is objected to because of the following informalities: Lines 5-6 of claim 1 include the phrase "using ***the a*** maximum modulation ratio…" (emphasis added). Appropriate correction is required.

5. Claim 9 is objected to because of the following informalities: The claim includes the term "comprisesing" in line 2 of the claim. The claim also includes a reference number "72" with respect to the re-ordering buffer in line 8. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 includes the limitation of “a channel decoder for…analyzing modulation methods for each sub-channels…” Claim 1 is directed towards an apparatus and the claim is written in a manner of a means clause (i.e. channel decoder) for performing a specified function (i.e. analyzing modulation methods for each sub-channels). The specification does not provide a description of the structure used to perform the function of "analyzing modulation methods for each sub-channels” therefore it is impossible to determine the equivalents of the element, as required by 35 U.S.C. § 112, sixth paragraph.

8. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Line 2 of claim 13 indicates the claim depends from the method of claim “121”. Examiner interprets this claim to depend from claim 12 since claim 12 is the only other method claim in the application.

Claim Rejections - 35 USC § 103

9. Claims 1 and 4-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Uesugi et al. (US 2002/0114379 A1), hereinafter "Uesugi".

Regarding claim 1, AAPA discloses a demodulation apparatus for receiving signals by an adaptive modulation and coding method, and demodulating the signals, in an OFDMA based packet communication system, comprising:

a QAM demapper for performing a QAM (Quadrature Amplitude Modulation) demapping process to the received signals **(Fig. 2, QAM Demapper 25)**;

a slot buffer for storing the data outputted from the QAM demapper for each slot **(Fig. 2, Slot Buffers 26; Para [10])**;

a channel decoder **(Fig. 2, Channel Decoder 27)** for decoding the data stored in the slot buffer **(Para [10])**, analyzing modulation methods for each sub-channels and transferring the analyzed modulation methods to the QAM demapper **(Para [11], [13])**; and reading valid data from the data stored in the slot buffer, based on the analyzed modulation methods for each sub-channels and demodulating the valid data, and outputting the demodulated data **(Para [10])**.

AAPA does not disclose demapping by a modulation method using the a maximum modulation ratio, and outputting data, until modulation methods for each sub-channels are analyzed.

Uesugi discloses demapping (i.e. demodulating) a received signal using the largest modulation level map **(Para [0094]; Figs. 3 and 4, Para [0060]-[0067] teaches demapping 64QAM with a 64QAM demodulation pattern; Figs. 5 and 6, Para [0068]-[0074] teaches demapping 16QAM with a 64QAM demodulation pattern; Figs. 7 and 8, Para [0076]-[0080] teaches demapping QPSK with a 64QAM demodulation pattern)**. Uesugi teaches that by demapping (i.e. demodulating) received QPSK and 16QAM signals using the 64QAM demodulation pattern (i.e. map) without any knowledge of the modulation scheme applied at the transmitter it is possible to decrease data delay **(Para [0095])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to demap (i.e. demodulate) signals using the maximum modulation ratio until the modulation methods for each sub-channels are analyzed because the teaching lies in Uesugi that this approach can decrease data delays.

Regarding claim 4, AAPA in view of Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein the slot buffer comprises:

a first slot buffer for storing data outputted from the QAM demapper until the modulation methods for each sub-channels of the received signals are analyzed by the channel decoder **(AAPA: Fig. 2, Slot Buffers 26, it would be obvious that the**

symbols demapped as taught by Uesugi could be stored in the Slot buffer of Fig. 2); and

a second slot buffer for storing data outputted from the QAM demapper, once the modulation methods for each sub-channels of the received signals are analyzed by the channel decoder **(AAPA: Fig. 2, Slot Buffers 26, (Fig. 2, Slot Buffers 26; Para [10], Para [11], Para [13])**.

Regarding claim 5, AAPA in view of Uesugi teaches the demodulation apparatus in the OFDMA based packet communication system of claim 4. It would have been merely a matter of obvious engineering design choice with respect to in which slot buffer illustrated in Fig. 2 of AAPA the demapped data is stored. Storing data demapped by the methods taught by Uesugi in one slot buffer and the data demapped by the conventional methods as taught by AAPA in a different slot buffer would not produce a new and unexpected result.

Regarding claim 6, AAPA in view of Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein the channel decoder reads the MAP information in the former part of a frame among the symbol data stored in the slot buffer, and analyzes the modulation methods for each sub-channels **(AAPA, Figs. 1-3, Para [10]-[11]; The Channel decoder 27 decodes data that passes through the slot buffers, and the MAP info is in the former part of the frame.)**.

Regarding claim 7, AAPA in view of Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein the

QAM demapper performs a demapping process to the received signals by the modulation methods for each sub-channels, and stores the output data in the slot buffer, once the modulation methods for each sub-channels are analyzed by the channel decoder **(AAPA, Para [10], [11], [13])**.

Regarding claim 8, AAPA in view of Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein in the case data are demodulated by the modulation method using the maximum modulation ratio, a constellation for part of the data are is identical with a constellation for the data demodulated by the modulation methods for each sub-channels **(Uesugi: Para [0094]; Figs. 3 and 4, Para [0060]-[0067] teaches demapping 64QAM with a 64QAM demodulation pattern)**.

Regarding claim 9, AAPA in view of Uesugi teaches the demodulation apparatus in the OFDMA based packet communication system of claim 8, wherein the demodulation apparatus further comprisesing:

an FFT unit for performing FFT (Fast Fourier Transform) to the received signals and outputting the signals **(AAPA; Fig. 2, FFT unit 21; Para [10])**;

a re-ordering buffer for re-ordering the signals outputted from the unit and storing the signals **(AAPA; Fig. 2, Reordering Buffers 22; Para [10])**;

an equalizer for estimating channels using the signals stored in the re-ordering buffer 72 and performing equalization of the signals, and outputting the signals to the QAM demapper **(AAPA; Fig. 2, Equalizer 23; Para [10])**.

Regarding claim 10, AAPA in view of Uesugi teaches the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein in the case the modulation method using the maximum modulation ratio is 64QAM, and a data unit for storing in the slot buffer is 6 bits of data **(Uesugi: Fig. 3)**; the valid data by the 16 QAM modulation method are former 4 bits of data from among the 6 bits of data **(Uesugi: Fig. 5, Para [0074])**.

Regarding claim 11, Uesugi teaches the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein in the case the modulation method using the maximum modulation ratio is 64 QAM, and data unit for storing in the slot buffer is 6 bits of data **(Uesugi: Fig. 3)**; the valid data by the QPSK modulation method are 2 bits of data in front of the 6 bits of data **(Uesugi: Fig. 5, Para [0080])**.

Regarding claim 12, AAPA discloses a demodulation method for receiving signals by an adaptive modulation and coding method and demodulating the signals, in an OFDMA based packet communication system, comprising stages of:

a) performing a demapping process to the received signals by a modulation method and storing the signals **(Fig. 2, QAM Demapper 25, Slot Buffer 26, Para [10])**;

b) decoding the demapped and stored signals the data and analyzing the modulation methods for each of sub-channels **(Fig. 2, Channel Decoder 27, Para [11])**; and

c) performing a demapping process on the received signals by the analyzed modulation methods for each sub-channels and demodulating the signals **(Para [13])**.

AAPA does not teach using a maximum modulation ratio for the demapping process.

Uesugi discloses demapping (i.e. demodulating) a received signal using the largest modulation level map **(Para [0094]; Figs. 3 and 4, Para [0060]-[0067] teaches demapping 64QAM with a 64QAM demodulation pattern; Figs. 5 and 6, Para [0068]-[0074] teaches demapping 16QAM with a 64QAM demodulation pattern; Figs. 7 and 8, Para [0076]-[0080] teaches demapping QPSK with a 64QAM demodulation pattern)**. Uesugi teaches that by demapping (i.e. demodulating) received QPSK and 16QAM signals using the 64QAM demodulation pattern (i.e. map) without any knowledge of the modulation scheme applied at the transmitter it is possible to decrease data delay **(Para [0095])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to demap (i.e. demodulate) signals using the maximum modulation ratio until the modulation methods for each sub-channels are analyzed because the teaching lies in Uesugi that this approach can decrease data delays.

10. Claims 2 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Uesugi, further in view of Matsumoto et al. (US 2002/0136207 A1), hereinafter "Matsumoto".

Regarding claim 2, the modification of AAPA with Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein the data demapped (i.e. demodulated) using the maximum modulation ratio results in varying amounts of valid data **(Fig. 3, six significant bits S0-S5; Fig. 5, four significant bits, S0-S3; Fig. 7, two significant bits S0-S1)**.

The combination of AAPA and Uesugi does not disclose controlling read enable signals for controlling the data output stored in the slot buffer.

Matsumoto teaches the use of read enable signals for accessing data from a buffer which is activated when a determination is made that the buffer contains valid data, and is deactivated when it is determined the data in the buffer is invalid **(Para [0093])**. Matsumoto suggests that in order to meet increasing demands on channel capacities and for higher speed channels, and improved buffer access method is required **(Para [0007]-[0008])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the buffer access methods taught by Matsumoto in the device taught by AAPA as modified by Uesugi in order to access valid data stored in a buffer by using a read enable signal because the suggestion lies in Matsumoto that this can result in higher speed data transfers.

Regarding claim 13, AAPA in view of Uesugi disclose the demodulation method in the OFDMA based packet communication system of claim 121 [*sic*], wherein

the signals are stored in stage a) until the modulation methods for each sub-channels are analyzed **(AAPA: Fig. 2, Slot Buffers 26, it would be obvious that the**

symbols demapped as taught by Uesugi could be stored in the Slot buffer of Fig. 2); and demodulating the valid data **(AAPA: Para [10])**

While Uesugi discloses the data demapped (i.e. demodulated) using the maximum modulation ratio results in varying amounts of valid data **(Fig. 3, six significant bits S0-S5; Fig. 5, four significant bits, S0-S3; Fig. 7, two significant bits S0-S1)**.

The combination of AAPA and Uesugi does not explicitly teach reading only valid data from among the signals are read by the modulation methods for each sub-channels analyzed in stage b).

Matsumoto teaches the use of read enable signals for accessing data from a buffer which is activated when a determination is made that the buffer contains valid data, and is deactivated when it is determined the data in the buffer is invalid **(Para [0093])**. Matsumoto suggests that in order to meet increasing demands on channel capacities and for higher speed channels, and improved buffer access method is required **(Para [0007]-[0008])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the buffer access methods taught by Matsumoto in the device taught by AAPA as modified by Uesugi in order to access the valid portion of the data acquired by the demapping process of Uesugi stored in a buffer by using a read enable signal because the suggestion lies in Matsumoto that this can result in higher speed data transfers.

11. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Uesugi, furthering view of Lassen et al. (US 2002/0087685 A1), hereinafter "Lassen".

Regarding claim 3, AAPA in view of Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1 wherein the data demapped (i.e. demodulated) using the maximum modulation ratio results in varying amounts of valid data **(Fig. 3, six significant bits S0-S5; Fig. 5, four significant bits, S0-S3; Fig. 7, two significant bits S0-S1)** but does not explicitly recite the limitation of claim 3.

Lassen teaches storing symbols in a temporary storage buffer **(Fig. 3, Decoder Temporary Storage Buffer 255)** prior to decoding. Lassen discloses the temporary storage can be faster access storage such as RAM in which the symbols are accessed from the RAM based on a schedule (i.e. valid data) **(Para [0241])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use RAM as taught by Lassen because the suggestion lies in Lassen that RAM provides faster memory access.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joey Bednash whose telephone number is (571)270-7500. The examiner can normally be reached on Mon-Fri 7:30 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Joey Bednash/
Examiner, Art Unit 2461

/Huy D Vu/

Supervisory Patent Examiner, Art Unit 2461